SCC #42 APPROVED 23 May 2000
MIL-STD-188-220B
Frame Check Sequence

5.3.4.2.5 Frame check sequence. For error detection, all frames shall include a 32-bit FCS prior to the closing flag sequence. The contents of the address, control, and information fields are included in the FCS calculation. Excluded from the FCS calculation are the 0's inserted by the 0-bit insertion algorithm. The formula for calculating the FCS, which is the 1's complement (inversion) of the remainder of a modulo-2 division process, employs the generator polynomial, P(X), having the form

$$P(x) = x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1$$

FCS generation shall be in accordance with the paragraph entitled "32-bit Frame Checking Sequence" in ISO 3309, and implemented in a manner that provides a unique remainder when a frame is received without bit errors incurred during transmission (Note: When the FCS is implemented via a 32 bit shift register, the shift register shall be initialized to all ones before checking or calculation of the FCS). If the FCS of a received frame proves the frame to be invalid, the frame shall be discarded.